Stability And Reliability Investigation on Fully ECL Compatible High Speed GaAs Logic ICs.

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Abstract

The electrical characteristics stability and reliability were investigated on newly developed high speed GaAs logic ICs. A resistor-loaded source-coupled FET logic (SCFL) was employed as a basic circuit architecture. The selectively epitaxial grown n^+ - GaAs layers were adopted for the contact regions of the WSi self-aligned gate FET. Maximum operating data rate of more than 2.6 Gb/s was achieved in these devices, guaranteeing sufficient supply voltage and phase margin. No failure has been observed in DC bias test for 3,000 hours and in RF operational test at 2 Gb/s for 7,000 hours.

I. Introduction

GaAs digital ICs have become increasingly important in high speed system applications such as high speed communication systems and measurement equipments in more than 2 Gb/s data rate area. As these ICs approaches being more practical, electrical characteristics stability, i.e., phase margin, supply voltage margin, tolerance on temperature variation, etc., as well as the device reliability become important.

However the complete investigations on above items have not yet been reported for high speed GaAs digital ICs.

This paper describes electrical characteristics and reliability on newly developed GaAs D-type flip flop (D-F/F), T-type flip flop (T-F/F) and 3-input OR-NOR Gate (3-in OR/NOR).

II. Circuit Design

In high speed systems, ECL (Emitter Coupled Logic) ICs are widely used. Thus full ECL compatibility, not only Input / Output logic levels but also supply voltages, is needed for GaAs digital ICs. To this end, a resistor-loaded source-coupled FET logic (SCFL)[1] was employed as a basic circuit architecture. Threshold voltage of the FET was optimized to be -0.2 V.

The D-F/F and T-F/F were constructed with a master-slave flip flop and output buffer circuits. Fig. 1 shows the equivalent circuit of the latch part in D-F/F. Reference voltages ($V_{REF.}$, $V_{CREF.}$) and current control bias voltage (V_{CS}) were internally generated, so that no additional external bias voltage are required for these ICs.

III. Device Fabrication

For FET fabrication, the sidewall-assisted technology was combined with WSi self-aligned FET technology. The epitaxial n^+ - GaAs layers were selectively grown[2] on the active layer in source and drain regions. Active layers for diodes, resistors and FETs were formed by selective Si ion implantation. A cross-sectional view of the FET is shown in Fig. 2. Typical

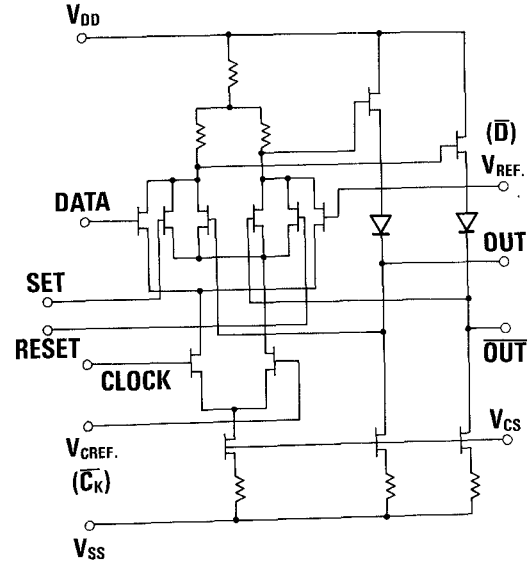

Fig. 1 Equivalent circuit for the latch part of the D-F/F.

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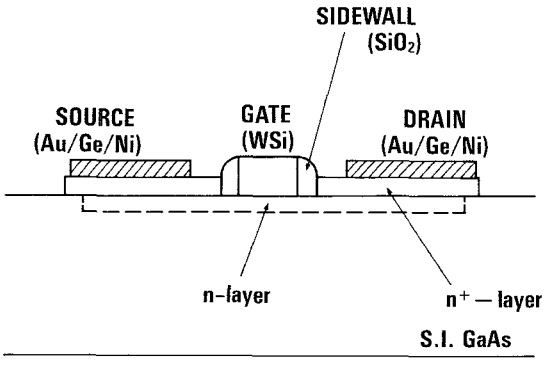


Fig. 2 Cross-sectional view of the FET.

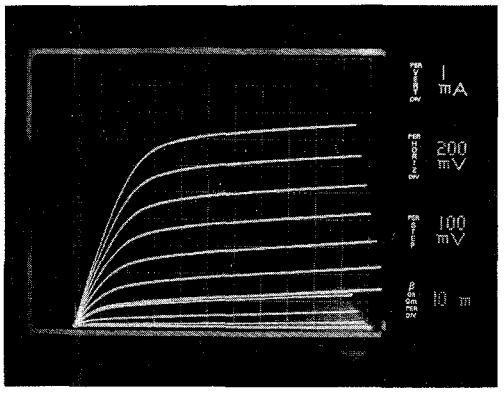


Fig. 3 Current-voltage characteristics of the FET.

(L_g = 0.8 um, W_g = 40 um, V_{th} = -0.3V)

current-voltage characteristics of an FET are shown in Fig. 3. An average g_m value of the 0.8 um long gate FET was typically 300 mS/mm at V_{GS} = +0.6 V, V_{DS} = 1 V.

The air-bridge wiring technique was employed to reduce the crossover capacitances. Figure 4 shows crossover capacitances with and without air-bridge. When the air-bridge technique was used, the crossover capacitance became about less than 1/10 compared with the conventional structure. SEM photograph of the air-bridge structure is shown in Fig. 5.

IV. Device Performance

Figure 6 shows the microphotograph of the D-F/F chip. The chip was packaged in 50-ohm matched 16-pin ceramic minuaturized flat-type package (Fig. 7).

A full ECL compatibility was successfully obtained with single supply voltage (V_{DD} = 0 V and V_{SS} = -5.2 V) without any external bias adjustment. Sufficiently large (1.0 V_{pp}) logic swing has been obtained at up to 3.2 Gb/s (Fig. 8).

From the practical viewpoint, tolerances in supply voltage (supply voltage margin) and in phase difference between input data signal and clock signal (phase margin) is important.

The examined phase margin and the supply voltage margin were for D-F/F at ambient temperatures of 25°C and 75°C as shown in Figs. 9 and 10, respectively. The maximum operating speed was 3.2 Gb/s. At up to 2.6 Gb/s, phase margin of more than 200 degrees and +5 % supply voltage margin were obtained at ambient temperature of up to 75°C. The high speed characteristics measurement was also carried out for T-F/F. A maximum toggle frequency of 5.0 GHz was obtained with full ECL compatibility. The 3-in OR/NOR showed output rise and fall times of about 100 ps (20 % to 80 %) and propagation delay time of 250 ps.

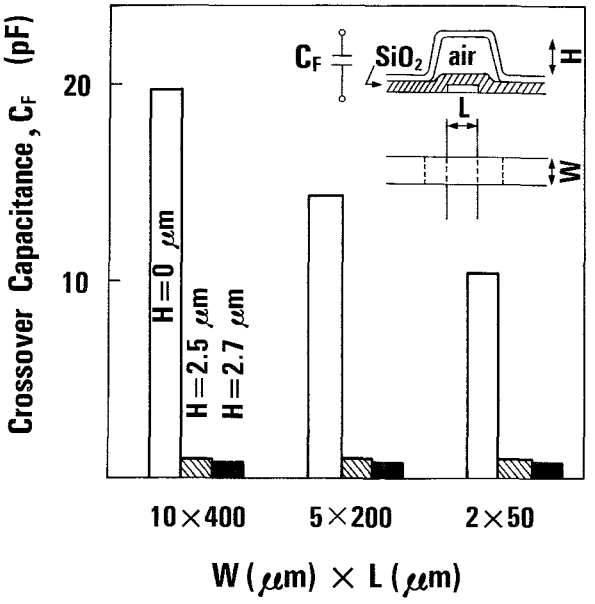


Fig. 4 Crossover capacitances with and without (H = 0 um) air-bridge.

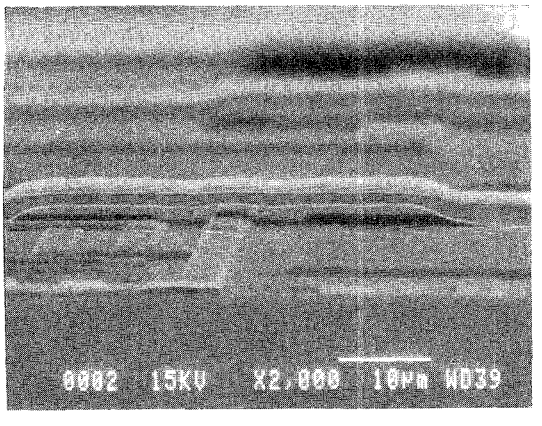


Fig. 5 SEM photograph of the air-bridge.

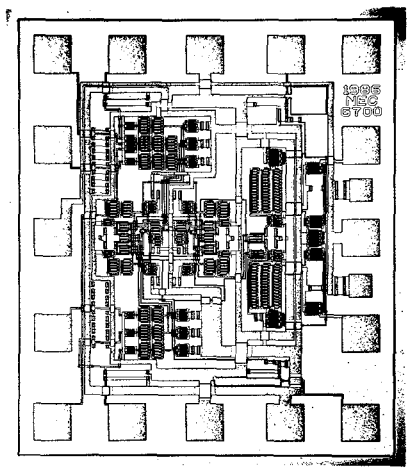


Fig. 6 Microphotograph of the D-F/F. (Chip size : 1.4 mm x 1.6 mm)

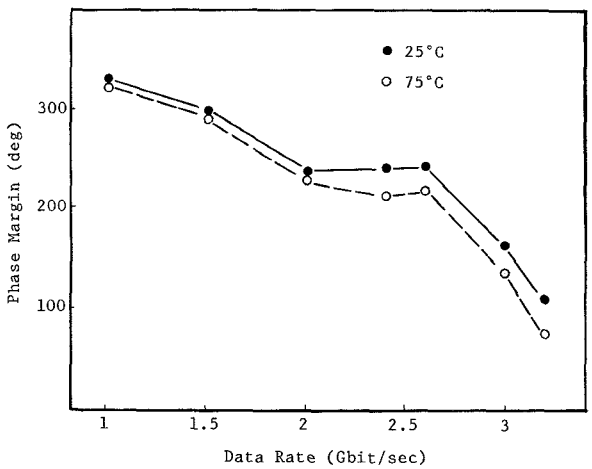


Fig. 9 Data rate dependence of D-F/F's phase margin.

V. Reliability

The reliability investigation for the present logic ICs were carried out on the following items.
(1) High temperature DC bias test (BT test).
(2) RF operational life test at 2 Gb/s for T-F/F.
(3) Thermal and mechanical environmental tests.

BT tests were carried out on D-F/F, T-F/F and 3-in OR/NOR under bias conditions of V_{DD} = 0V, V_{SS} = -5.2 V at T_{Ch} of 220°C. Sample numbers were 10 for each ICs.

The variation of circuit current (I_{DD}), output pulse rise time (t_r) and output pulse fall time (t_f) of the T-F/F were shown in Fig. 11. At present (3,000 hours), no failure has been observed within ±10 % criteria in each ICs.

RF operational life test were carried out on 10 T-F/F under the conditions of V_{DD} = +2 V, V_{SS} = -3.2 V and f = 2 Gb/s at T_{Ch} = 54°C. No failure has been observed at 7,000 hours. The variation of I_{DD}, t_r and t_f were shown in Fig. 12.

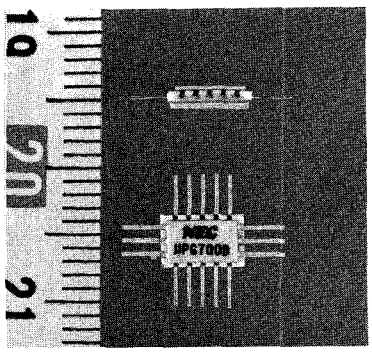
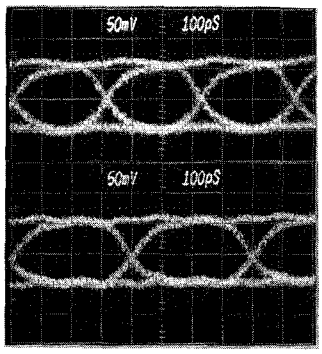


Fig. 7 Overall photograph of 50-ohm matched package for GaAs logic ICs.



at 3.2 Gb/s

at 2.5 Gb/s

Div. (Hori.) = 100 ps
Div. (Vert.) = 500 mV

Fig. 8 Output waveforms of the D-F/F.

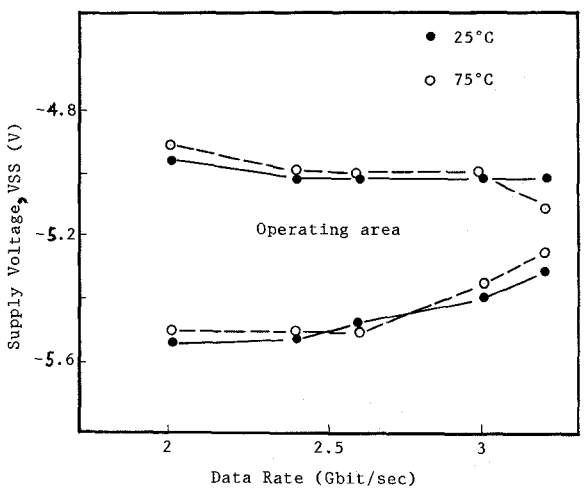


Fig. 10 Data rate dependence of D-F/F's supply voltage margin.

Figure 13 shows output waveforms of T-F/F at 2 Gb/s for the initial and after 7,000 hours test devices. Lastly, the thermal and mechanical environmental tests based on MIL-STD-883 were carried out on T-F/F and no failure was observed.

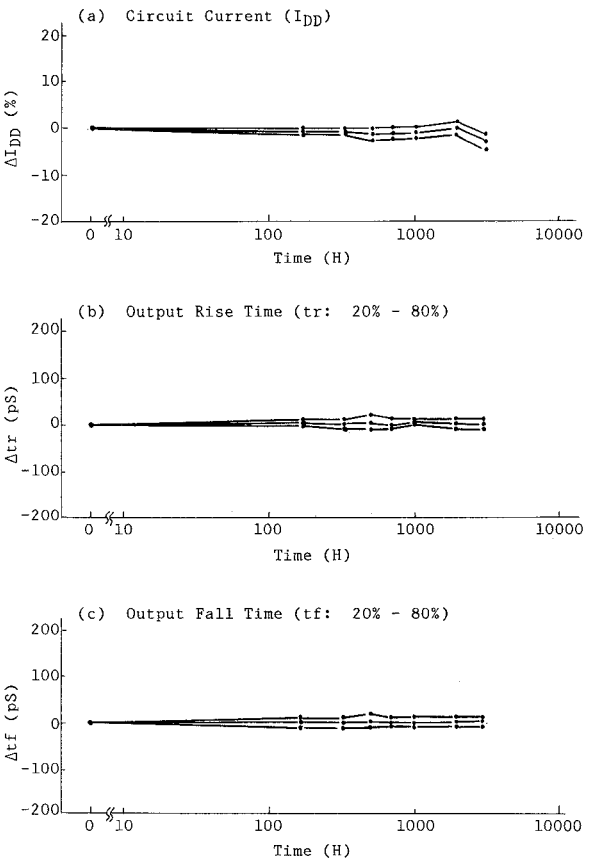
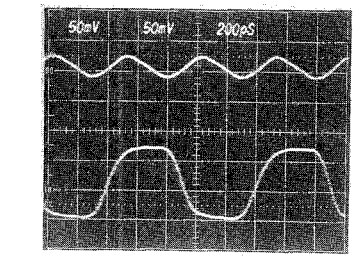


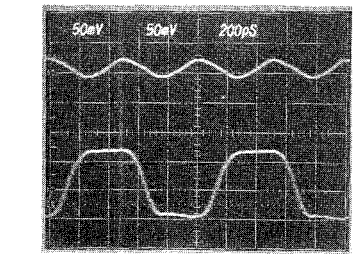
Fig. 11 Variations of I_{DD}, t_r and t_f in T-F/F BT tests.



Data input

Data output

initial



Data input

Data output

after 7,000 hours test

Div. (Hori.) = 200 ps
Div. (Vert.) = 500 mV

Fig. 13 Output waveforms of T-F/F at 2 Gb/s.

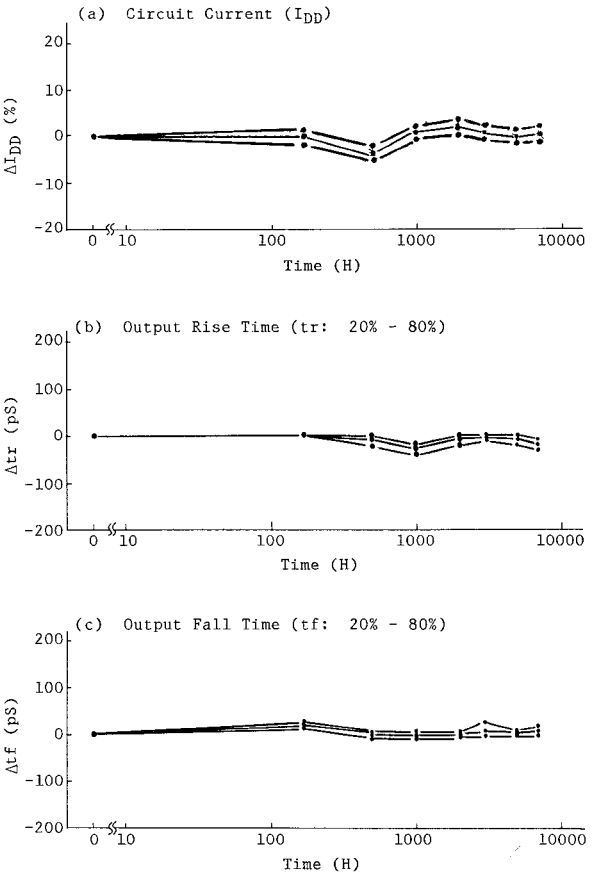


Fig. 12 Variations of I_{DD}, t_r and t_f in T-F/F RF operational tests.

VI. Conclusion

The stability and reliability study has been carried out on high Speed GaAs digital ICs. The present device exhibited more than 2.6 Gb/s operating speed, guaranteeing sufficient supply voltage and phase margin with high reliability.

VII. Acknowledgement

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